What is claimed is:

1. A sensor for electrostatic discharge (ESD) protection, comprising:

a voltage divider coupled to an input terminal of the sensor, wherein a voltage drop occurs across the voltage divider and a high state voltage is generated at an output terminal of the sensor when the input terminal of the sensor is coupled to an ESD voltage pulse; and

a device coupled to the voltage divider, wherein the device is adapted to maintain the high state voltage at the output terminal of the sensor, while the input terminal of the sensor is coupled to the ESD voltage pulse.

2. The sensor of claim 1, wherein the input terminal of the sensor is coupled to a voltage supply terminal.

3. The sensor of claim 1, wherein the voltage divider comprises a series of diodes.

4. The sensor of claim 3, wherein the series of diodes has about 3 to about 8 diodes.

5. The sensor of claim 1, wherein the device comprises a metal-oxide-semiconductor (MOS) transistor.

6. The sensor of claim 5, wherein the MOS transistor of the device is a N-type MOS (NMOS) transistor.

7. The sensor of claim 6, wherein a gate terminal and a drain terminal of the NMOS transistor are common.

8. The sensor of claim 1, wherein the output terminal of the sensor is coupled to an inverter.

9. The sensor of claim 8, wherein the inverter is coupled to an ESD circuit.

10. The sensor of claim 9, wherein the inverter is coupled to a gate terminal of a MOS transistor of the ESD circuit.

11. The sensor of claim 10, wherein the MOS transistor of the ESD circuit is a cascaded NMOS.

12. The sensor of claim 11, wherein the gate terminal of the MOS transistor is pulled down to a low state voltage when the input terminal of the sensor is coupled to the ESD voltage pulse.

13. A circuit for electrostatic discharge (ESD) protection, comprising:

an ESD protection circuit having a metal-oxide-semiconductor (MOS) transistor with a gate terminal therein ;

a sensor that senses an ESD pulse and generates a high state voltage at an output terminal of the sensor in response to the ESD pulse; and

an inverter coupled to the output terminal of the sensor and the ESD circuit.

14. The circuit of claim 13, wherein the gate terminal of the MOS transistor of the ESD circuit is pulled down to a low state voltage by an output voltage of the inverter when the sensor senses the ESD pulse.

15. The circuit of claim 13, wherein the sensor comprises:

a voltage divider coupled to an input terminal of the sensor, wherein a voltage drop occurs across the voltage divider and a high state voltage is generated at an output terminal of the sensor when the input terminal of the sensor is coupled to a voltage generated by the ESD pulse; and

a device coupled to the voltage divider, wherein the device is adapted to maintain the high state voltage at the output terminal, while the input terminal of the sensor is coupled to the ESD voltage pulse.

16. The circuit of claim 15, wherein the input terminal of the sensor is coupled to a voltage supply terminal.

17. The circuit of claim 15, wherein the voltage divider comprises a series of diodes.

18. The circuit of claim 17, wherein the series of diodes has about 3 to about 8 diodes.

19. The circuit of claim 15, wherein the device comprises a metal-oxide-semiconductor (MOS) transistor.

20. The circuit of claim 19, wherein the MOS transistor of the device is a N-type MOS (NMOS) transistor.

21. The circuit of claim 20, wherein a gate terminal and a drain terminal of the NMOS transistor of the device are common.

22. The circuit of claim 13, wherein the MOS transistor of the ESD circuit is a cascaded NMOS.

23. A method for electrostatic discharge (ESD) protection, comprising:

sensing an ESD pulse; and

pulling down a gate terminal of a MOS transistor of an ESD circuit to a low state voltage when the ESD pulse is sensed.

24. The method of claim 23, wherein the step of sensing the ESD pulse is performed by a sensor.

25. The method of claim 24 further comprising connecting the sensor to a voltage supply terminal to sense the ESD pulse.

26. The method of claim 25 further comprising generating a high state voltage at an output terminal of the sensor when the ESD pulse is sensed.

27. The method of claim 26 further comprising connecting the output terminal of the sensor to an inverter to generate a low state voltage at an output terminal of the inverter when the ESD pulse is sensed.

28. The method of claim 27 further comprising connecting the output terminal of the inverter to the gate terminal of the MOS transistor of the ESD circuit.